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APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
10/586,507	07/17/2006	Clemens Gerhardus Johannes De Haas	NL04 0061 US1	4614

65913 7590 04/28/2008

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EXAMINER	
HILTUNEN, THOMAS J	

ART UNIT	PAPER NUMBER
2816	

NOTIFICATION DATE	DELIVERY MODE
04/28/2008	ELECTRONIC

Please find below and/or attached an Office communication concerning this application or proceeding.

The time period for reply, if any, is set in the attached communication.

Notice of the Office communication was sent electronically on above-indicated "Notification Date" to the following e-mail address(es):

ip.department.us@nxp.com

Office Action Summary	Application No.	Applicant(s)	
	10/586,507	DE HAAS, CLEMENS GERHARDUS JOHANNES	
	Examiner	Art Unit	
	Thomas J. Hiltunen	2816	

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) OR THIRTY (30) DAYS, WHICHEVER IS LONGER, FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133). Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

1)☒ Responsive to communication(s) filed on *17 July 2006*.

2a)☐ This action is **FINAL**. 2b)☒ This action is non-final.

3)☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

4)☒ Claim(s) *1-9* is/are pending in the application.

4a) Of the above claim(s) _____ is/are withdrawn from consideration.

5)☐ Claim(s) _____ is/are allowed.

6)☒ Claim(s) *1-5,8 and 9* is/are rejected.

7)☒ Claim(s) *6 and 7* is/are objected to.

8)☐ Claim(s) _____ are subject to restriction and/or election requirement.

Application Papers

9)☐ The specification is objected to by the Examiner.

10)☒ The drawing(s) filed on *17 July 2006* is/are: a)☐ accepted or b)☒ objected to by the Examiner.

Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).

Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).

11)☐ The oath or declaration is objected to by the Examiner. Note the attached Office Action or form PTO-152.

Priority under 35 U.S.C. § 119

12)☐ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).

a)☐ All b)☐ Some * c)☐ None of:

1.☐ Certified copies of the priority documents have been received.

2.☐ Certified copies of the priority documents have been received in Application No. _____.

3.☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

Attachment(s)

1) ☒ Notice of References Cited (PTO-892)
2) ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)
3) ☐ Information Disclosure Statement(s) (PTO/SB/08) Paper No(s)/Mail Date _____.
4) ☐ Interview Summary (PTO-413) Paper No(s)/Mail Date. _____.
5) ☐ Notice of Informal Patent Application
6) ☐ Other: _____.

DETAILED ACTION

Drawings

The drawings are objected to because figures 1 and 2 disclose blank boxes with no label/detail (i.e., 13, 16 of Fig. 1 and 13, 16, 19, 23, 26, 29, 20, 206, 208a and 208b of Fig. 2) the blank boxes should be labeled. Furthermore, every claimed limitation must be shown in the drawings. Thus, "a substrate arrangement coupled to the power supply reference conductor" as recited in claim 1 must be shown. Corrected drawing sheets in compliance with 37 CFR 1.121(d) are required in reply to the Office action to avoid abandonment of the application. Any amended replacement drawing sheet should include all of the figures appearing on the immediate prior version of the sheet, even if only one figure is being amended. The figure or figure number of an amended drawing should not be labeled as "amended." If a drawing figure is to be canceled, the appropriate figure must be removed from the replacement sheet, and where necessary, the remaining figures must be renumbered and appropriate changes made to the brief description of the several views of the drawings for consistency. Additional replacement sheets may be necessary to show the renumbering of the remaining figures. Each drawing sheet submitted after the filing date of an application must be labeled in the top margin as either "Replacement Sheet" or "New Sheet" pursuant to 37 CFR 1.121(d). If the changes are not accepted by the examiner, the applicant will be notified and informed of any required corrective action in the next Office action. The objection to the drawings will not be held in abeyance.

Claim Rejections - 35 USC § 102

The following is a quotation of the appropriate paragraphs of 35 U.S.C. 102 that form the basis for the rejections under this section made in this Office action:

> A person shall be entitled to a patent unless –
>
> (b) the invention was patented or described in a printed publication in this or a foreign country or in public use or on sale in this country, more than one year prior to the date of application for patent in the United States.

Claims 1-3, 8 and 9 are rejected under 35 U.S.C. 102(b) as being anticipated by Ausserlechner et al. (USPN 6,559,721).

With respect to claim 1, Ausserlechner et al. discloses in Figs. 2 and 10, an electronic circuit, comprising a signal conductor (OUT), a power supply reference conductor (VDD) and a switching circuit (P1 and N1) coupled between the signal conductor (OUT) and the power supply reference conductor (VDD), the switching circuit comprising:

a substrate arrangement (nSUB and Sn, see Fig. 4) coupled to the power supply reference conductor (nSUB is connected to VDD, see Col. 7 lines 34-37);

a first MOS transistor (P1) realized on said substrate arrangement (Sn, see Fig. 4) with a source, a drain and a gate, the source being coupled to the power supply reference conductor (VDD), the first MOS transistor (P1) having a first conductivity type (PMOS);

a second MOS transistor (N1) realized on said substrate arrangement (Sn, see Fig. 4) with a source, a drain and a gate, the source being coupled to the drain of the first MOS transistor (when the transistors P1 and N1 become conductive, i.e., are turned on, then their respective source and drains will be connected together through

the source to drain conduction paths of each transistor device. Furthermore, in CMOS technology there is no structural difference between the drain and source of a MOS transistor, thus a source of a transistor is the same as a drain of a transistor), the drain being coupled to the signal conductor (the drain of N1 is connected to OUT), the second MOS transistor (N1) having a second conductivity type opposite the first conductivity type (NMOS);

a control circuit (PA, CP1, CP2) with outputs coupled to the gate of the first MOS transistor (A1 coupled to G1) and the gate and source of the second MOS transistor (output of CP1 to G2, CP1 is coupled to the source of N1, since CP1 is coupled to the Vdd terminal, which is coupled to the source of N1 via P1. Thus CP1 is coupled to the source and gate of N1), the control circuit being arranged to switch between an "on" state and an "off "state, in which the control circuit controls the gate source voltages of the first and second MOS transistor to make channels of these MOS transistors conductive and not to make the channels of these first and second transistors conductive respectively (the control circuit signals output to the gates of P1 and N1 control the gate source voltages of P1 and N1 thus turning P1 and N1 on and off).

With respect to claim 2, Ausserlechner et al. discloses, an electronic circuit according to claim 1, comprising a further power supply reference conductor (GND) and a further switching circuit (N2 and P2), complementary to the switching circuit, the further switching circuit comprising:

a third MOS transistor (N2) of the second conductivity type (NMOS), having a source, a drain and a gate, the source being coupled to the further power supply reference conductor (GND);

a second MOS transistor (P2) of the first conductivity type (PMOS), with a source, a drain and a gate, the source being coupled to the drain of the third MOS transistor (when the transistors P2 and N2 become conductive, i.e., are turned on, then their respective source and drains will be connected together through the source to drain conduction paths of each transistor device. Furthermore, in CMOS technology there is no structural difference between the drain and source of a MOS transistor, thus a source of a transistor is the same as a drain of a transistor), the drain being coupled to the signal conductor (OUT) or a further signal conductor;

the control circuit (PA and CP2) having outputs coupled to the gate of the third MOS transistor (A2 coupled to G4 of N2) and the gate and source of the fourth MOS transistor (CP2 is coupled to the gate of P2, i.e., G3, and the source of P2 through N2, since CP2 is coupled to GND wherein the source of P2 is coupled to GND through N2. Thus, CP2 is coupled to the source of P2 via N2), the control circuit applying gate source voltages to the third and fourth MOS transistor to make these third and fourth MOS transistors conductive and not to make these transistors conductive respectively (the control circuit signals output to the gates of P1 and N1 control the gate source voltages of P1 and N1 thus turning P1 and N1 on and off).

With respect to claim 3, Ausserlechner et al. discloses, an electronic circuit according to claim 2, wherein the control circuit (PA, CP1 and CP2) is arranged to

supply first substantially matching gate-source voltages to the first and fourth MOS transistor and second substantially matching gate-source voltages to the second and third MOS transistor (PA outputs symmetrical voltages A1 and A2. Similarly, CP1 and CP2 output two symmetrical signals that are shifted 3 Volts above VDD and below GND, respectively. Thus, the gate to source voltages of P1 and P2 will be substantially the same with respect to logic value, i.e., both transistors will be activated by low voltages, and the of the gate to source voltages of N1 and P2 will have substantially the same logic level, i.e., both will be activated by high voltage levels. Furthermore, there is no explicitly recited definition of "substantially matching" within the claims. Thus, the 3 Volt offset at the output of CP1 and CP2 is "substantially matching" in that both P1 and P2 are active low and N1 and N2 are active high).

With respect to claim 8, Ausserlechner et al. discloses in Fig. 2 and 4, an electronic circuit, comprising a signal conductor (OUT), a first and second power supply conductor (VDD, GND), a first switching circuit coupled between the first power supply conductor and the signal conductor (P1 and N1) and a second switching circuit coupled between the second power supply conductor and the signal conductor (N2 and P2) or a further signal conductor (202), the first switching circuit comprising:

a first PMOS transistor (P1) with a source, a drain and a gate, the source being coupled to the first power supply conductor (VDD);

a first NMOS transistor (N1) with a source, a drain and a gate, the source being coupled to the drain of the first PMOS transistor (when the transistors P1 and N1 become conductive, i.e., are turned on, then their respective source and drains will be

connected together through the source to drain conduction paths of each transistor device. Furthermore, in CMOS technology there is no structural difference between the drain and source of a MOS transistor, thus a source of a transistor is the same as a drain of a transistor), the drain being coupled to the signal conductor (the drain of N1 is connected to OUT), the drain being coupled to the signal conductor (OUT);

the second switching circuit comprising:

a second NMOS transistor (N2) with a source, a drain and a gate, the source being coupled to the second power supply conductor (GND);

a second PMOS transistor (P2) with a source, a drain and a gate, the source being coupled to the drain of the second NMOS transistor (when the transistors P2 and N2 become conductive, i.e., are turned on, then their respective source and drains will be connected together through the source to drain conduction paths of each transistor device. Furthermore, in CMOS technology there is no structural difference between the drain and source of a MOS transistor, thus a source of a transistor is the same as a drain of a transistor), the drain being coupled to the signal conductor (the drain of N1 is connected to OUT), the drain being coupled to the signal conductor (OUT) or the further signal conductor (202); the electronic circuit comprising:

a control circuit (PA, CP1, and CP2) with outputs coupled to the gate of the first PMOS transistor (A1 coupled to G1), the gate of the second NMOS transistor (A2 coupled to G4), the gate and source of the first NMOS transistor (output of CP1 coupled to the gate of N1, CP1 is coupled to the source of N1, since CP1 is coupled to VDD and the source of N1 is coupled to VDD via P1) and the gate and source of the second

PMOS transistor (CP2 coupled to the gate of P2, CP2 is coupled to the source of P2, since CP2 is coupled GND and the source of P2 is coupled to ground via N2), the control circuit being arranged to switch between an "on" state and an "off "state, in which the control circuit controls the second NMOS transistor to make channels of these transistors conductive and not to make the channels of these first and second transistors conductive respectively (the control signals output to the gates of P1, N1, P2 and N2 control the gate source voltages of each respective transistor to turn each transistor on and off)..

With respect to claim 9, Ausserlechner et al. discloses, an electronic circuit according to claim 8, wherein the control circuit is arranged to supply first substantially matching gate-source voltages to the first and second PMOS transistor and second substantially matching gate-source voltages to the first and second NMOS transistor (PA outputs symmetrical voltages A1 and A2. Similarly, CP1 and CP2 output two symmetrical signals are shifted 3 Volts above VDD and below GND, respectively. Thus, the gate to source voltages of P1 and P2 will be substantially the same with respect to logic value, i.e., both will be activated by low voltages, and the of the gate to source voltages of N1 and P2 will have substantially the same logic level, i.e., both will be activated by high voltage levels. Furthermore, there is no explicitly recited definition of "substantially matching" within the claims. Thus, the 3 Volt offset at the output of CP1 and CP2 is "substantially matching" in that both P1 and P2 are active low and N1 and N2 are active high).

Claim Rejections - 35 USC § 103

The following is a quotation of 35 U.S.C. 103(a) which forms the basis for all obviousness rejections set forth in this Office action:

> (a) A patent may not be obtained though the invention is not identically disclosed or described as set forth in section 102 of this title, if the differences between the subject matter sought to be patented and the prior art are such that the subject matter as a whole would have been obvious at the time the invention was made to a person having ordinary skill in the art to which said subject matter pertains. Patentability shall not be negatived by the manner in which the invention was made.

Claims 1, 4 and 5 are rejected under 35 U.S.C. 103(a) as being unpatentable over Tanzawa (USPAPN 2003/0151945) in view of Doyle, III (USPN 4,710,730).

With respect to claim 1, Tanzawa discloses in Figs. 9 and 10, an electronic circuit, comprising a signal conductor (Vddh), a power supply reference conductor (21) and a switching circuit (QN1, QP1, QN2) coupled between the signal conductor (Vddh) and the power supply reference conductor (21), the switching circuit comprising:

a substrate arrangement (substrate, i.e. back gate, of QP1) coupled to the power supply reference conductor (the substrate, i.e., back gate, of QP1 is coupled to 21 via QN1);

a first MOS transistor (QN1) with a source, a drain and a gate, the source being coupled to the power supply reference conductor (21, when QN1 is conductive its source is connected to 21), the first MOS transistor (QN1) having a first conductivity type (NMOS);

a second MOS transistor (QP1) realized on said substrate arrangement with a source, a drain and a gate, the source being coupled to the drain of the first MOS transistor (when the transistors QN1 and QP1 become conductive, i.e., are turned on, then their respective source and drains will be connected together through the source to

drain conduction paths of each transistor device. Furthermore, in CMOS technology there is no structural difference between the drain and source of a MOS transistor, thus a source of a transistor is the same as a drain of a transistor), the drain being coupled to the signal conductor (the drain of QP1 is connected to Vddh), the second MOS transistor (QP1) having a second conductivity type opposite the first conductivity type (PMOS);

a control circuit (26-29) with outputs coupled to the gate of the first MOS transistor (27 coupled to QN1) and the gate and source of the second MOS transistor (the output of regulator 29 is coupled to the source and gate of QP1, see Fig. 10, which discloses the output of the regulator, i.e., node connected between QP2 and PN5, is connected to the gate of QP1 and the source of QP1, i.e., the source of the QP1 is connected to the gate of QP1 via the diode connected transistor QP2), the control circuit being arranged to switch between an "on" state and an "off "state, in which the control circuit controls the gate source voltages of the first and second MOS transistor to make channels of these MOS transistors conductive and not to make the channels of these first and second transistors conductive respectively (the control circuit controls the activation of QN1 and QP1 by controlling their respective gate source voltages).

Note while Fig. 1 discloses the prior art being composed on a P substrate, Tanzawa fails to specifically both the first and second transistors being composed on a single substrate. However, it is old and well known to compose all of the elements of an integrated circuit on the same substrate to cause the devices to track more closely over

temperature and process variations thus increasing the accuracy of the integrated circuit. This is further evidenced by Doyle, III (USPN 4,710,730) in Col. 4 lines 6-9.

It would have been obvious to one of ordinary skill in the art at the time of the invention to construct all the elements, including the first and second transistors of Fig. 9 and 10, of the integrated circuit of Tanzawa on the same semiconductor substrate to cause the devices of the integrated circuit to "track more closely over temperature and processing variations" as disclosed by Doyle, III to further increase the accuracy/performance of the circuit of Fig. 9 and 10 Tanzawa.

With respect to claim 4, Tanzawa discloses, an electronic circuit according to claim 1, wherein the control circuit comprises:

a power supply input (input to charge pump 43 of Fig. 10) for supplying a power supply voltage with a first polarity relative to the power supply reference conductor (Vddh, which is essentially equal to the voltage at the supply conductor), the first conductivity type being such that the channel of the first MOS transistor (QN1) becomes conductive when a voltage at its gate has a second polarity (Boosted Vddh), opposite the first polarity relative to its source (the source of QN1 is coupled to ground via QP1, PN2, R1 and R2. Thus, QN1 is activated by a high voltage reference opposite that of the low voltage reference of ground connected to R2);

a pump circuit (43) fed with the power supply voltage (Vddh) and arranged to generate the gate voltage of the first MOS transistor with the second polarity relative to the power supply reference conductor in the "on" state (QN1 is activated with the charge pump outputs a high boosted voltage).

With respect to claim 5, Tanzawa discloses, an electronic circuit according to claim 1, wherein the control circuit comprises: a

power supply input (input to charge pump 43 of Fig. 10) for supplying a power supply voltage relative to the power supply reference conductor (Vddh, which is essentially equal to the voltage at the supply conductor) with a first polarity (supply voltage), the second conductivity type being such that the channel of the second MOS transistor becomes conductive when a voltage at its gate has a second polarity opposite the first polarity relative to its source (the gate of QP1 is low, i.e. opposite of Vddh, QP1 is activated);

a resistive element (QP2, which is a resistive element since all circuit devices have an inherent resistance) coupled between the gate and source of the second MOS transistor (QP2 is connected between that gate and source of QP1); a current source circuit (QN5) coupled between the power supply input and the gate of the second MOS transistor (the drain of QN5 is coupled to the gate of QP1 and the gate of QN5 is coupled to Vddh via R1), for supplying a predetermined, state dependent current from the power supply input to through the resistive element (QP2 outputs a regulated, i.e., predetermined, signal to the gate of QP1).

Allowable Subject Matter

Claims 6 and 7 are objected to as being dependent upon a rejected base claim, but would be allowable if rewritten in independent form including all of the limitations of the base claim and any intervening claims.

With respect to claim 6, there is no cited art that discloses a second resistor element and a current mirror connected as recited and being connected to the resistive element, the power supply reference conductor, the further power supply reference conductor and second MOS transistor of the circuit as recited in claims 1 and 5. Claim 7 is allowable for at least the same reasons as claim 6.

Cited Art

Wada et al. (USPN 6,487,133) discloses a switching circuit (12 and 13) in Fig. 2 similar to the one recited in claim 1.

Lee et al. (USPN 6,661,253) discloses in Col. 1 lines 32-34 that is well-known that is no difference between the "drain" and "source" terminal of a MOS device.

Conclusion

Any inquiry concerning this communication or earlier communications from the examiner should be directed to Thomas J. Hiltunen whose telephone number is (571)272-5525. The examiner can normally be reached on M-F 8:00am - 4:30pm.

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Drew Richards can be reached on (571)272-1736. The fax phone number for the organization where this application or proceeding is assigned is 571-273-8300.

Information regarding the status of an application may be obtained from the Patent Application Information Retrieval (PAIR) system. Status information for published applications may be obtained from either Private PAIR or Public PAIR. Status information for unpublished applications is available through Private PAIR only. For more information about the PAIR system, see http://pair-direct.uspto.gov. Should you have questions on access to the Private PAIR system, contact the Electronic Business Center (EBC) at 866-217-9197 (toll-free). If you would like assistance from a USPTO Customer Service Representative or access to the automated information system, call 800-786-9199 (IN USA OR CANADA) or 571-272-1000.

TH
April 17, 2008

/N. Drew Richards/
Supervisory Patent Examiner, Art Unit 2816